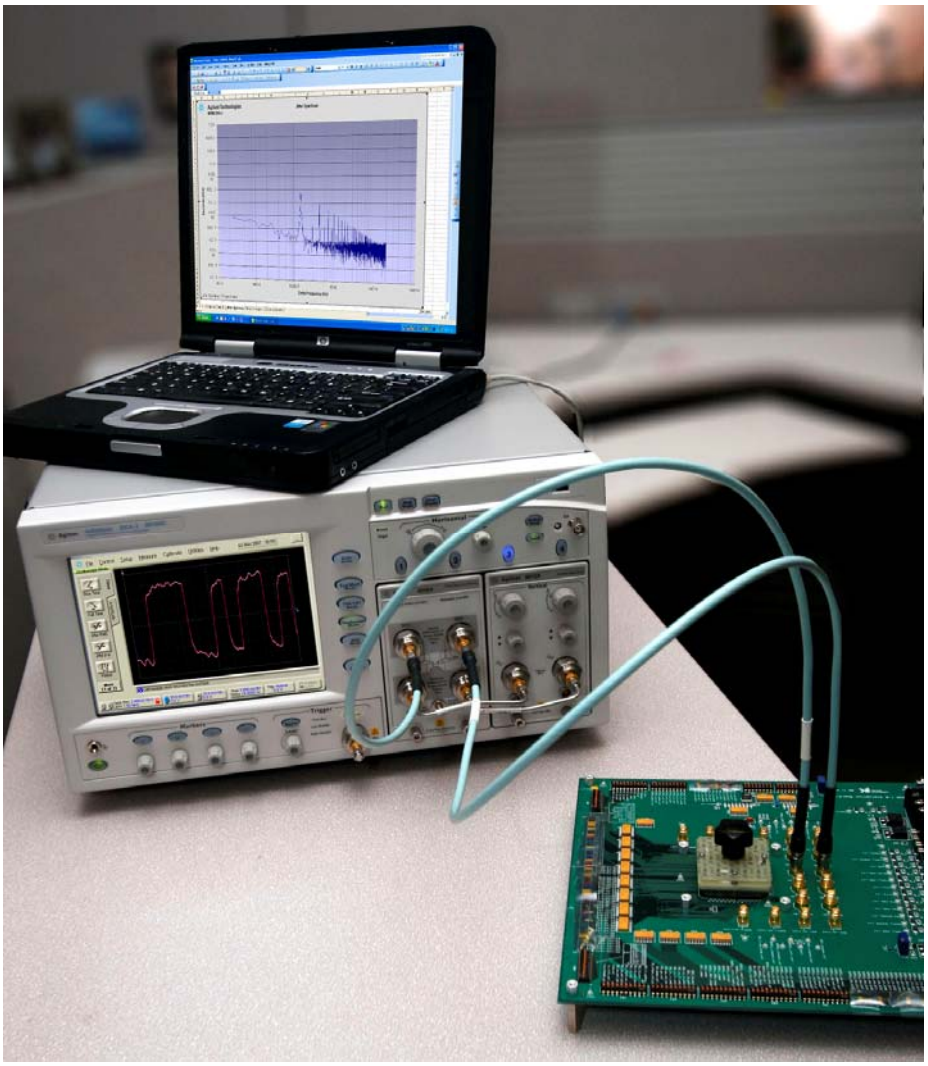
Operation Guide: Using the 86100C DCA-J Jitter Spectrum and Phase Noise Application Revision 1.0

I Overview

The Jitter Spectrum and Phase Noise (JSPN) Application is based on a Microsoft Excel spreadsheet which controls the instrument and performs the required calculations on the acquired data. A technical review of the importance of these measurements and how they provide insight into the root causes of jitter is provided in Agilent Product Note 86100C-2 **"Solving Jitter Problems Through Jitter Spectrum and Phase Noise Analysis"**

The only supported use model is one where the Excel spreadsheet is not running on the internal PC of the 86100C mainframe. A separate computer runs the application and is connected to the DCA-J through the GPIB port. The easiest and most common approach is to run the JSPN Application on a laptop computer connected to the DCA-J GPIB port through a USB to GPIB adapter as shown below:



The USB to GPIB adapter is available through Agilent Technologies as part number 82357A or B (www.agilent.com)

This operating guide will explain:

- Control Computer hardware and software requirements
- 86100C DCA-J configuration requirements
- Where to get the application software
- How to load the application software on the control computer
- How to connect the control computer to the 86100C DCA-J
- How to connect the DUT to the 86100C DCA-J
- How to lock the 83496B Clock Recovery Module
- How to setup the JSPN application
- How to run the JSPN application and interpret the results

II Hardware Requirements

Computer requirements:
Available hard drive space – 100 Megabytes
RAM – 500 Megabytes
Processor – 1GHz or faster

Instrument Requirements:
86100C DCA-J with firmware 7.0 or higher. (Note the application will not work with 86100A or B mainframes)
83496B or 83496UAB clock recovery module with any options in either slot (left is default). Note that the application will not operate with the 83496A clock recovery

module, but an 83496A can be upgraded to an 83496UAB. Contact your local Agilent representative for details.
82357A or USB/GPIB interface (easiest method to connect PC to 86100C) or equivalent:

	Agilent Hardware			National Instruments Hardware*		
	82350B GPIB interface PCI card.	82357A or B GPIB to USB converter.	E5810A LAN/GPIB Gateway	PCI-GPIB	USB/GPIB	LAN/GPIB Gateway GPIB-ENET/100
Windows 2000						
Excel 2000		✓				
Excel 2003						✓
Excel 2007	☒	☒	☒	☒	☒	☒
Windows XP						
Excel 2000						
Excel 2003		✓		✓		✓
Excel 2007	☒	☒	☒	☒	☒	☒
Windows Vista						
Excel 2000		☒				
Excel 2003		☒				
Excel 2007	☒	☒	☒	☒	☒	☒

✓	Tested Configurations
	Not tested but expected to work
☒	No Windows Vista driver for Agilent 82357 USB/GPIB
☒	Not compatible

* NI hardware, but requires Agilent IO libraries to be installed.

III Software requirements

PC Operating System – Windows 2000 or XP

Microsoft Excel 2000 or 2003 (as of May 2007 the application will not run on Microsoft Office 2007 or on Microsoft Vista). The application requires Analysis ToolPak and the Analysis ToolPak – VBA.. To confirm those tools are loaded, start Excel on the control computer and look under Tools-->Add-Ins. Make sure boxes are checked for each of these add-ins.
Agilent IO libraries (see Agilent.com "IO libraries)

IV Getting and Installing the Application Software

The JSPN Application software is currently available from Agilent Technologies free of charge as a web download by following these instructions:

1. Go to www.agilent.com/find/dcaj and look for the link to the Jitter Spectrum and Phase Noise application and follow the instructions for download

Alternatively

1. Go to the Agilent web site, www.agilent.com
2. Search for the 86100C by placing "86100C" in the search window and clicking "enter"
3. Go the 86100C web page
4. Click on "Jitter Spectrum and Phase Noise Application" and follow the instructions for download

V Connecting the Control Computer to the 86100C DCA-J

1. If using a USB to GPIB converter:
   a. Install the drivers that come with the USB to GPIB converter
   b. Install the manufacturer's provided VISA libraries
   c. Connect the USB plug to a USB port on the computer
   d. Connect the GPIB plug to the GPIB port on the 86100C mainframe
2. If using a GPIB card in the control computer
   a. Install the GPIB card and load the driver per manufacturer's instructions
   b. Install the manufacturer's provided VISA libraries
   c. Connect the GPIB cable between the GPIB port on the control computer and the GPIB port on the 86100C

VI Connecting the DUT to the 86100C DCA-J and locking the Clock Recovery Module

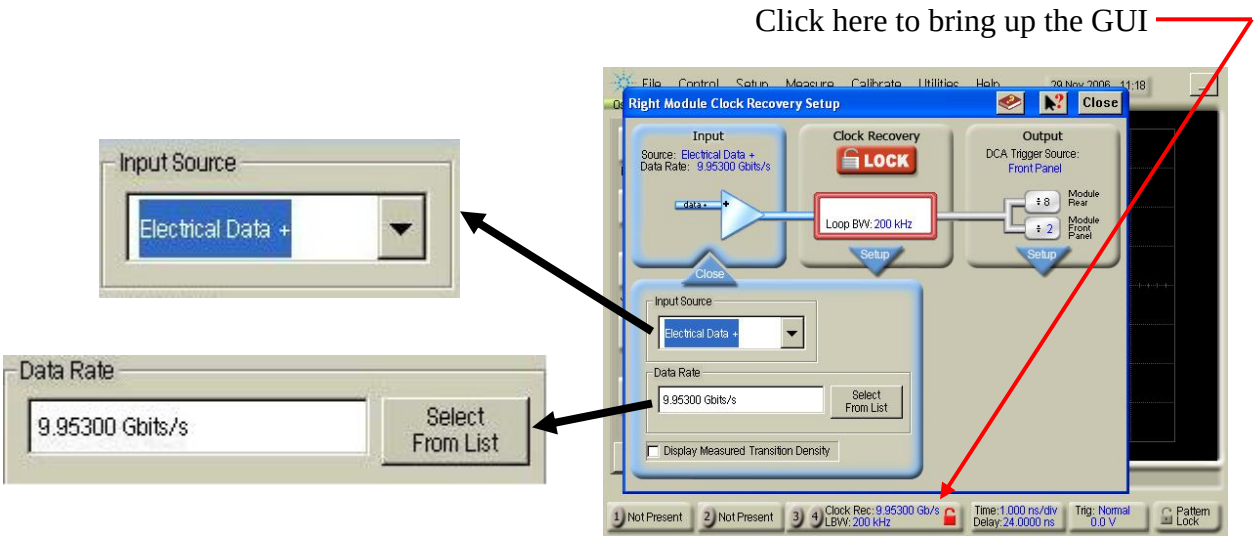
One of the unique capabilities of the 86100C DCA-J JSPN Application is that it can measure the jitter spectrum and phase noise on both clock and data signals. All that is required is the 83496B clock recovery module be able to lock on the signal.

Connect the signal to be tested from the DUT to the appropriate input of the 83496B:

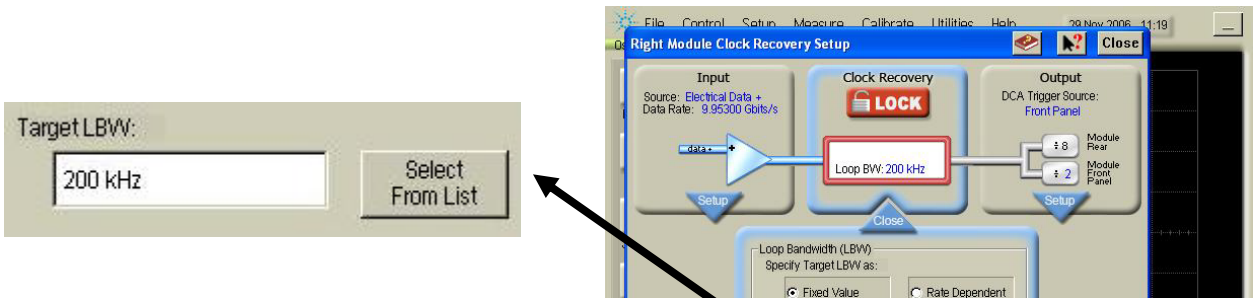
- Data+ or DATA– input for single ended electrical signals
- Data+ and DATA- inputs for differential electrical signals
- 9/125um input for single mode optical signals with wavelength of 1250-1620 nm
- 62.5/125 um input for multi-mode optical signals with wavelength of 780 to 1330 nm

The 86100C DCA-J on-line help explains, in detail, how to use the 83496B clock recovery module. Below is a brief outline of how to lock the 83496B clock recovery module to the incoming signal. Refer to on-line help if more details are needed:

- Verify your signal is in the data rate range your 83496B can support (50 Mbits/s to 7.1 Gbits/s for "standard" 83496B modules, 50 Mbits/s to 13.5 Gbits/s for 83496B modules with option 200). If you need to evaluate a signal below 50 Mbits/s see Appendix C.
- In the 83496B user interface (GUI), set the clock recovery input source to the input that is connected to the DUT (optical, data+, data- or differential).
- Set the data rate to the data rate of your incoming signal. Note that the clock recovery module treats all input signals as if they are data, even if the signal is actually a clock. That means if your signal is actually a clock, the 83496B will "see" this signal as a 101010 data pattern at a data rate that is double the clock rate. Thus to measure a clock signal, you must "convert" the clock frequency to a data rate (data rate = 2 X clock frequency). As an example, the "data rate" for a typical 100 MHz PCI Express reference clock is entered as 200 Mbits/s. This brings up an important point. The range of clock frequencies that can be measured by the system is half the range of data rates that can be measured. For example, when an 83496B option 200 is used, the data rate range is 50 Mb/s to 13.5 Gb/s. The effective clock rate range that can be tested is 25 MHz to 6.75 GHz.



- Since you will get the best (lowest noise) jitter spectrum and phase noise measurement at the narrowest loop bandwidth setting, set the loop bandwidth to the minimum (you can increase this if needed to lock). If you do not know the minimum loop bandwidth setting for the data rate you are using, enter 1 kHz and the 86100C DCA-J software will automatically go to the narrowest loop bandwidth setting available at the data rate you have chosen.



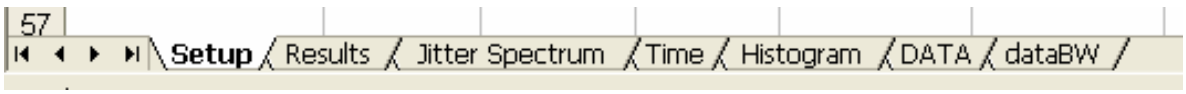
- Touch or click on the red "lock" icon to lock the clock recovery module to the input signal.
- If the clock recovery module does not lock to the input signal you may need to increase the loop bandwidth setting. To test this, enter the maximum loop bandwidth setting for the data rate you are using. If you do not know the maximum loop bandwidth setting for the data rate you are using, enter 10 MHz and the 86100C DCA-J software will automatically go to the widest loop bandwidth setting available at the data rate you have chosen.
- Try to lock again. If you still cannot lock there is a problem in the setup that is likely to be independent of the loop bandwidth. If you can lock with the widest loop bandwidth setting, reduce the loop bandwidth and try to re-lock. Continue to experiment until you are locked at the narrowest loop bandwidth setting possible. (Note that part of the JSPN application injects a step function into the loop in order to characterize its own loop dynamics. It is possible that in some circumstances injecting that small step can cause the loop to fall out of lock. If that happens, increasing the loop bandwidth by 10% should correct the problem).

Note that once the JSPN application has been run, it effectively places the 86100C mainframe under remote control. The instrument will not respond to front panel control unless the front panel LOCAL key has been pressed.

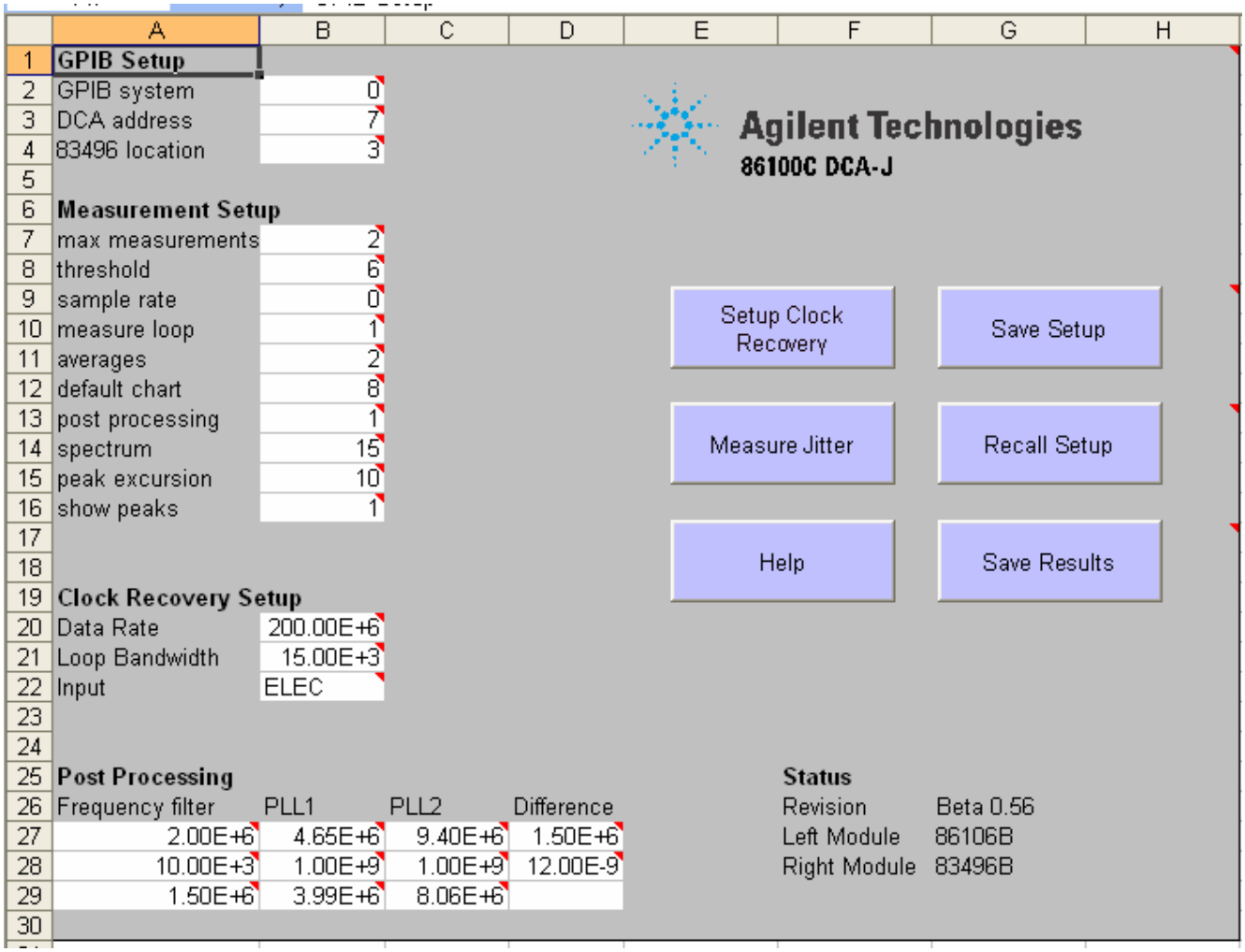
VII Setting-up the jitter spectrum and phase noise measurement

A. Application Setup

Open the Jitter spectrum and phase noise Application spreadsheet and go to the "SETUP" tab:



The following page will be displayed which shows the user interface for the application. This is used to configure the measurement as well as control the instrumentation:



The left side of the page is where the measurement system is configured including remote control addressing, how the measurement will be performed, and definitions for post processing algorithms. The right side of the setup page includes the control panel to initiate the measurement process and controls to save results and customized setups.

Note that in most cells that allow the user to manipulate the entry, a "tool tip" is provided to document what should be entered and what the typical entries should be. Simply place the cursor over the cell to enable the tool tip. No mouse 'click' is required to launch the tool tip

	A	B	
1	**GPIB Setup**		
2	GPIB system	0	
3	DCA address	7	
4	83496 location	3	
5			
6	**Measurement Setup**		
7	max measurements	2	
8	threshold	6	
9	sample rate	0	
10	measure loop	1	
11	averages	2	
12	default chart	8	
13	post processing	1	
14	spectrum	15	
15	peak excursion	10	
16	show peaks	1	
17			
18			
19	**Clock Recovery Setup**		
20	Data Rate	200.00E+6	
21	Loop Bandwidth	15.00E+3	
22	Input	ELEC	
23			
24			
25	**Post Processing**		
26	Frequency filter	PLL1	Pl
27	2.00E+6	4.65E+6	
28	10.00E+3	1.00E+9	
29	1.50E+6	3.99E+6	
30			

1 **GPIB setup**: Three entries define the addressing for how the computer communicates to the 86100C mainframe and 83496B clock recovery module:

(a) *GPIB system* =: enter the address of the GPIB card that is connected to the 86100C mainframe in this location
(b) *DCA address* =: enter the 86100C DCA-J GPIB address in this location
(c) *83496 location* =: enter the slot where the 83496B is installed
  (i) 1 for the left slot
  (ii) 3 for the right slot.

2 Measurement Setup

(a) *Max measurements:* Sets the maximum number of phase noise measurements the system will make before processing and displaying the results. This effectively sets the number of acquisitions that will be obtained before the system process the data and displays the averaged result for all acquisitions. It is similar to setting the averaging factor for general oscilloscope waveform acquisition. Note that if the threshold value is exceeded (described below), the instrument will present the results before the prescribed number of waveforms have been obtained.
(b) *Threshold*: This allows control of when data is saved and displayed. This parameter is based on the magnitude of the phase error at the output of the 83496B phase detector. When the magnitude of the error signal exceeds threshold value multiplied by the standard deviation of the error signal, the system will stop acquiring data and display the results. Thus the threshold value can stop acquisition prior to when the "max measurement" setting has been achieved. If the threshold value is never observed, the measurement will stop when the "max measurement" value has been met. When set to 0, each phase measurement will be recorded. For information on using this feature to capture a phase transient or glitch, see Appendix A below.
(c) *Sample rate*: This selects the sample rate of the internal acquisition system.
  (i) 0= 40Ms/S. This setting enables measurement of the highest frequency jitter spectrum and phase noise possible (3 kHz to 20 MHz offset)
  (ii) 64 = 4 Ms/S. This setting enables measuring as close to the carrier as possible (300 Hz to 2 MHz offset).
(d) *Measure Loop*: This controls whether or not the loop response of the 83496B clock recovery module, having been locked to the signal being evaluated, will be measured. In most applications this should be set to 1 so the loop response will be measured. This then allows the system to compensate for the loop response and provide accurate results. If multiple measurements are to be made with a specific signal such that the 83496B

is not required to relock, earlier loop measurements are valid and the loop need not be re-measured. The setting can be 0. Note that if the data rate changes, or the pattern of a data signal changes, the loop should be measured to account for these changes.

(e) *Averages:* This sets the number of measurements that are taken in the characterization of the loop bandwidth of the 83496B system and is generally not altered by the user. Note that this does not control how many measurements are acquired on the test signal (achieved with the max measurement parameter) and is only used as part of the test system characterization

(f) *Default Chart:* This sets the priority for the charts that will be displayed. 5 is for the time display, 6 for the histogram display, and 8 for the jitter spectrum display. Regardless of the priority setting, all test results will be available by selecting the appropriate spreadsheet page. This control simply dictates which page will be displayed first.

(g) *Post processing:* The measurement results can be further analyzed by processing them through a virtual network composed of two PLL's and a transport delay. The network is user definable. 1 enables post processing, 0 disables post processing. See "**Post Processing**" below

(h) *Spectrum:* The system has the ability to display results from different "points of view" including the signal at the input to the 83496B (setting 15), the signal observed after passing through the dual-PLL post processing function (setting 12, See "**Post Processing**" below), or the phase error observed at the output of the 83496 phase detector (setting 3)

(i) *Peak Excursion, Show Peaks:* The jitter spectrum and phase noise displays may contain spectral lines when periodic jitter is present. It can be useful to determine the actual energy for these periodic tones. In the jitter spectrum plot, spectral tones are displayed in seconds versus frequency. Markers can be placed on these tones and when the computer cursor is placed on one of these markers, the signal level can be displayed. The marker will read out the jitter magnitude in seconds rms. The marker function will display the "center of mass" of the signal, which may be composed of multiple trace points. In the phase noise display, energy is displayed as the signal power normalized to a 1 Hz bandwidth relative to the carrier power. While this is useful for a noise spectrum, it can be problematic for spectral tones. Trace markers are designed to show the total signal power of the tone relative to the carrier, without being normalized to a 1 Hz bandwidth. This is similar to how periodic modulation is displayed on a spectrum analyzer. Thus the peak markers will be located at the x-axis position of the tone, but will be placed several dB higher than the trace peak position. The marker readout is thus a dBc value rather than a dBc/Hz value. When there are many discrete jitter tones, the ability to control when markers are placed and when they are not can prevent a cluttered display. This is achieved with the "peak excursion" and the "show peaks" parameters. The "show peaks" enables (1) or disables (0) the placement of markers. The "peak excursion" value

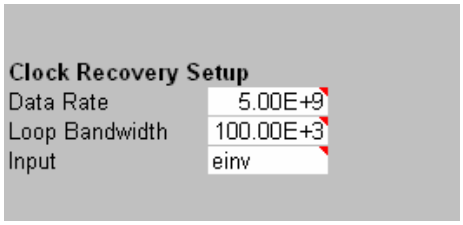
sets the minimum ratio of the signal to noise floor to receive a marker. When the value is large, only very prominent spectral lines will be marked.

3 To setup averaging in the frequency domain – See Appendix B

4 Glitch Capture Mode (Advanced) Settings – See Appendix A

B. Clock Recovery Setup

Note that several parameters for the 83496B clock recovery module can be controlled through the JSPN application or through the 86100CC mainframe user interface to the 83496B. The values entered into the JSPN application will override the manual settings made through the mainframe. To control the 83496 through the application, there are three entries available on the main setup page: Data rate, loop bandwidth, and input port. On the main setup page there is a section for clock recovery setup:



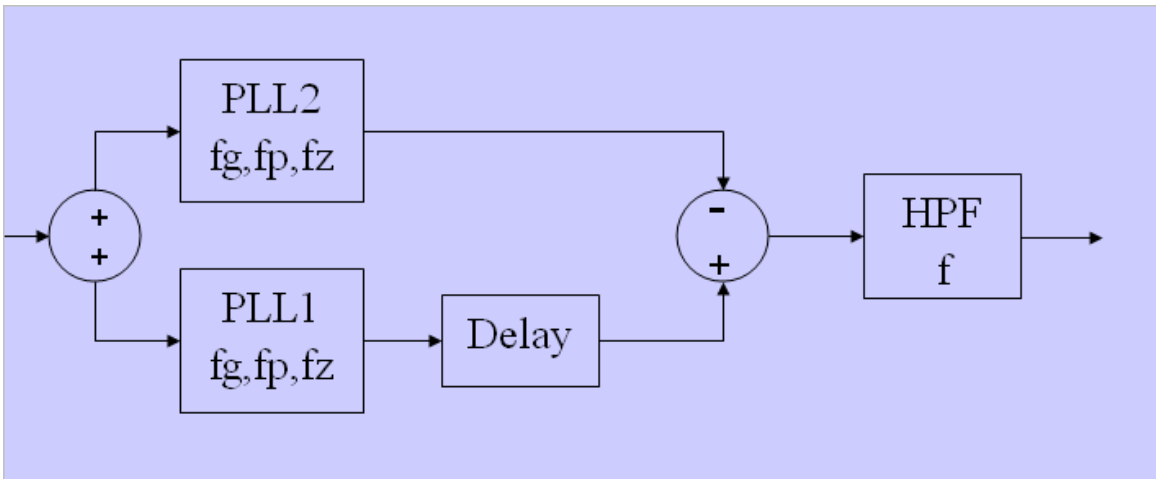
1 Set Data Rate
   (a) Click the "Data Rate" entry cell
   (b) Enter the data rate (as determined in section VI above) in the data rate block and press Enter on the PC keyboard
2 Set Loop Clock recovery Loop Bandwidth
   (a) Click the "Loop Bandwidth" entry cell
   (b) Enter the loop bandwidth (as determined in section VI above) in the loop bandwidth block and press enter on the PC keyboard.
3 Configure the input port:
   (a) Click the Input entry cell
   (b) Enter the Input port on the 83496B that is receiving the test signal: ELEC for the positive data port, EINV for the inverted data port, DIFF when using both electrical ports, and OPT for the optical port (83496B option 101)

Once the clock recovery has been setup, the clock recovery hardware needs to be synchronized to the incoming signal. Press the "Setup Clock Recovery" key on the main setup page:

The JSPN application will perform a lock sequence on the test signal on the 83496B. (If the signal does not lock, verify that the settings match the test signal. You can also verify manually that the 83496B is capable of locking to the signal by operating the system from the 86100C mainframe front panel. Verify that the mainframe is in LOCAL mode by pressing the mainframe LOCAL key. The oscilloscope can also be used to verify the quality of the signal. If a reasonable waveform cannot be displayed, it may not be possible to perform a jitter spectrum/phase noise test).

Post Processing

The JSPN measurement results can be manipulated with a user defined network composed of two third-order PLLs, a transport delay, and a high-pass filter as shown below:



The main reason for this feature is to implement the PCI-Express difference function, which is designed to assess the impact of the jitter of a signal as it would be seen by a receiver. Since the PCI-Express system uses a distributed clock, there will be a delay term altering the phase of the receiver clock relative to the phase of the clock used at the transmitter. Also, the PPL bandwidths of the transmitter and the receiver will not be identical. Thus when the reference clock jitter is measured, rather than determine its absolute performance, the signal is processed through a virtual network representing the PCI-Express system.

The virtual network is defined in the post processing section of the Setup page. There are 8 parameters that can be defined:

For PLL1 there is a gain term (the frequency at which the PLL has unity gain), a pole frequency, and a zero frequency for a third order PLL model. For PLL2, similar gain frequency, pole frequency, and gain frequency parameters are entered. All values should be entered in Hertz. The difference function is defined by a high-pass filter frequency (in units of Hertz and a time difference accounting for the transport delay between the two PLLs is entered (in seconds). (Note that each cell has notation which is made visible by placing the cursor over the cell, indicating what parameter it accepts).

24				
25	**Post Processing**			
26	Frequency filter	PLL1	PLL2	Difference
27	2.00E+6	4.65E+6	9.40E+6	1.50E+6
28	10.00E+3	1.00E+9	1.00E+9	12.00E-9
29	1.50E+6	3.99E+6	8.06E+6	
30				

The PCI-Express equations can be defined in terms of natural frequency and damping factor. Also, the PLL's can be second order rather than third order. To create a second order PLL, the pole frequency (second entry for each PLL) can be set to a large value, such as 1 GHz). To determine the gain and zero frequency entries from natural frequency and damping factor, the following equations are used:

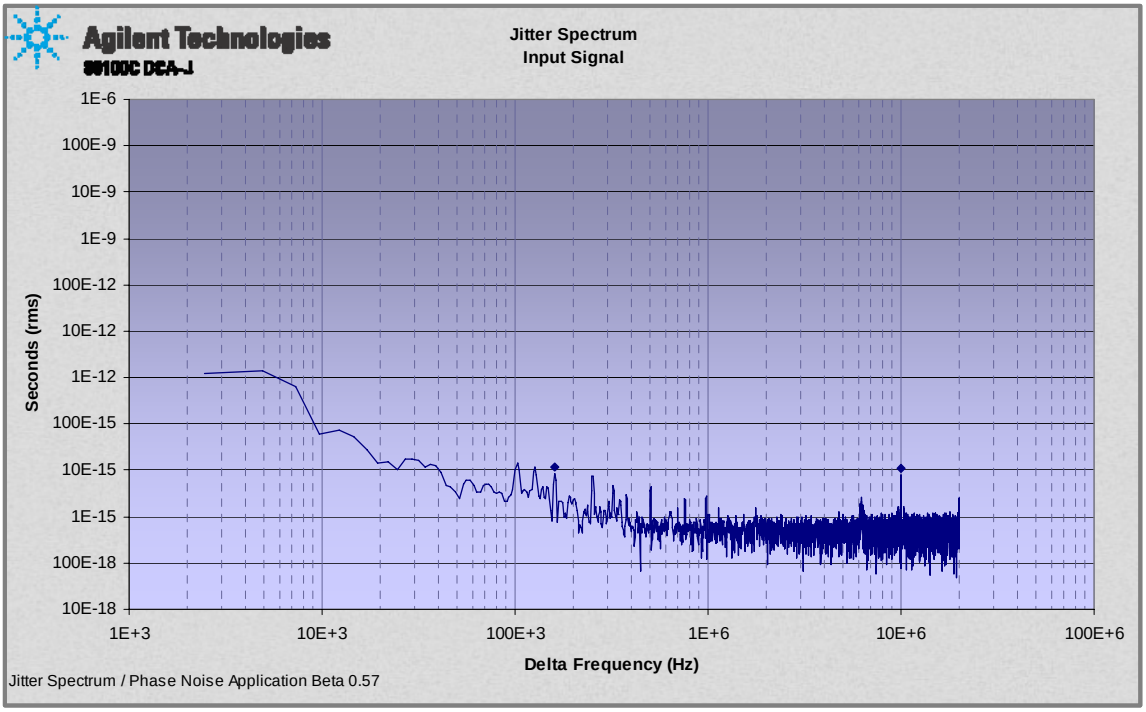
Gain frequency = natural frequency*damping factor*2

Zero frequency = Natural frequency/(2*damping factor)

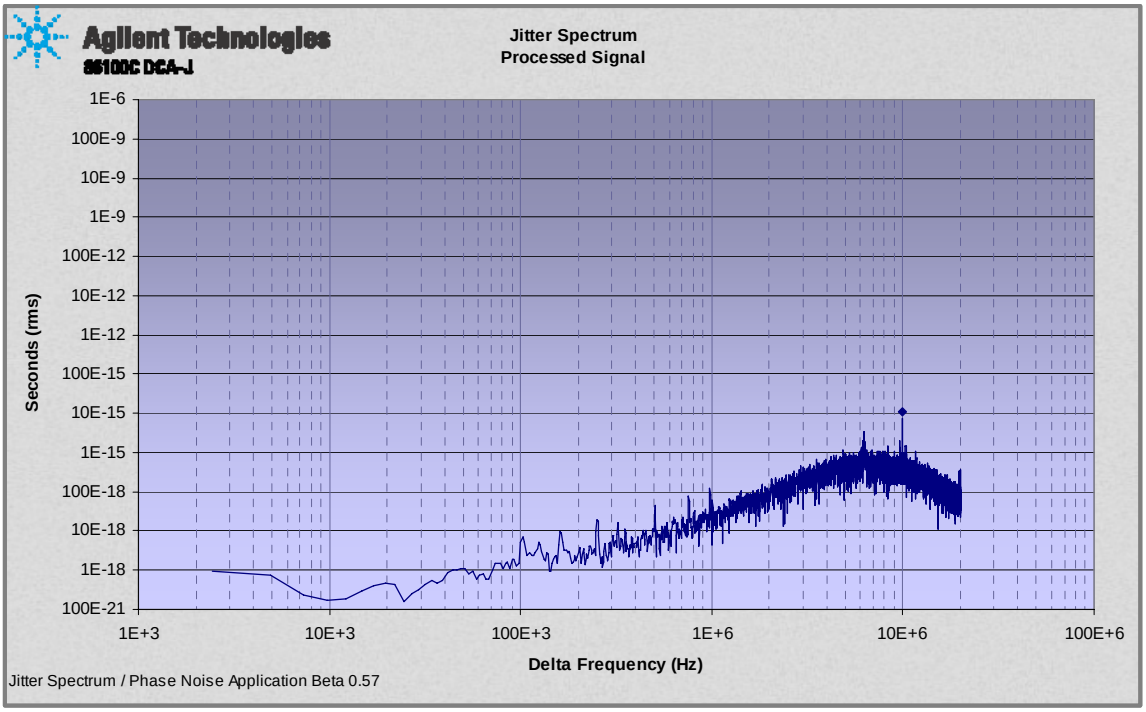
Post processing using the virtual network is enabled by setting the post processing cell in the measurement setup to 1. A 0 value disables the post processing. When enabled, the following measurements are made with the virtual network in place:

Jitter spectrum
Phase Noise spectrum
Jitter versus time
Frequency versus time
Jitter histogram (note that the jitter histogram is only available when post processing is enabled)

The following two measurements of a 2.5 GHz clock are made without and then with the virtual PLL system:



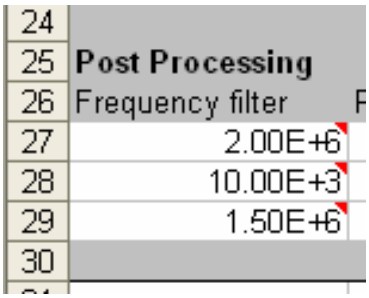
Clock jitter spectrum with no post-processing



Clock jitter spectrum with post-processing through the virtual PLL network

Note that in the second jitter spectrum plot that the low frequency jitter is significantly reduced through the high-pass effect of the virtual PLL's.

The frequency versus time display is generated by differentiating the measured phase. Since frequency is the derivative of phase, and differentiation can sometimes generate artificial noise, a low-pass filter is available to smooth out this effect. The jitter spectrum can be processed to determine random, deterministic, and total jitter. The range of the spectrum to be processed is defined by the user through two filter settings. These filter settings for the spectral integration are also user-definable in the setup page under the post processing section.



There are three "frequency filter" parameters that can be entered. The first is the low pass cutoff frequency used in the jitter versus time display. The second and third settings are for two filters that define the bandwidth for the jitter integrations. The allowable range of the frequency values is from 300 Hz to 2 MHz (when the sample rate is 40 MS/s) or 3 kHz to 20 MHz (when the sample rate is set to 40 MS/s.

Random jitter is determined through integration of the jitter spectrum, with the spectral tones removed, over three different bandwidths. The first is from the first filter frequency to the maximum frequency of the measurement (either 2 or 20 MHz, depending on the sample rate setting). The second bandwidth is from second filter frequency to the maximum frequency. The third bandwidth is the frequency range between the two filter settings.

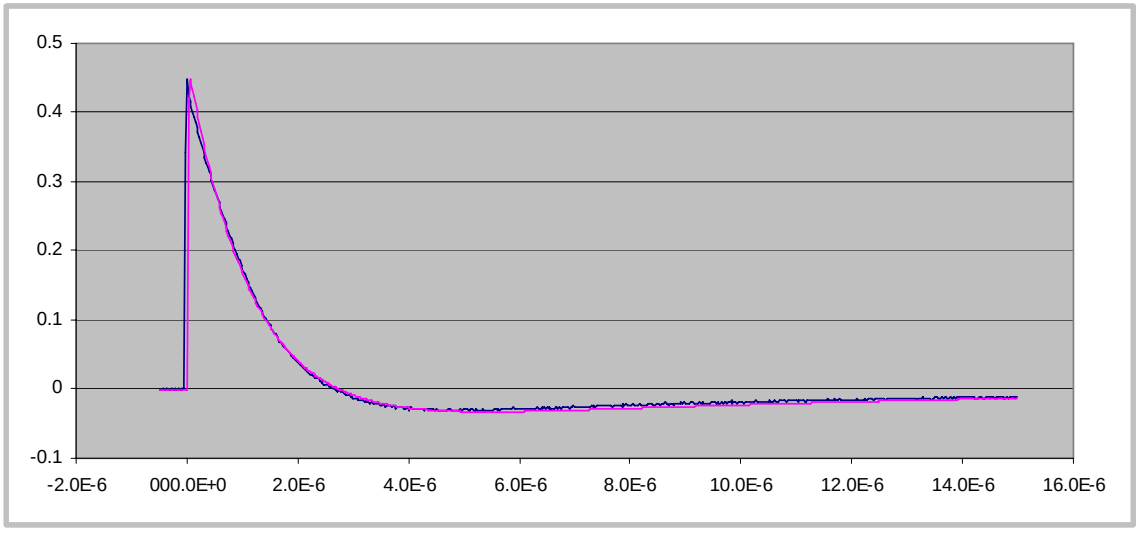
Deterministic jitter is determined over similar ranges. It is determined by taking the rms sum of all the spectral peaks of the jitter spectrum. Note that the user has control over the definition of what is determined to be a spectral peak, which can influence this result.

Total jitter is determined by performing an RMS integration of the complete spectrum over the integration limits defined by the user.

VIII Measuring jitter spectrum and phase noise

A. Click the "Measure Jitter" button while on the main SETUP page.

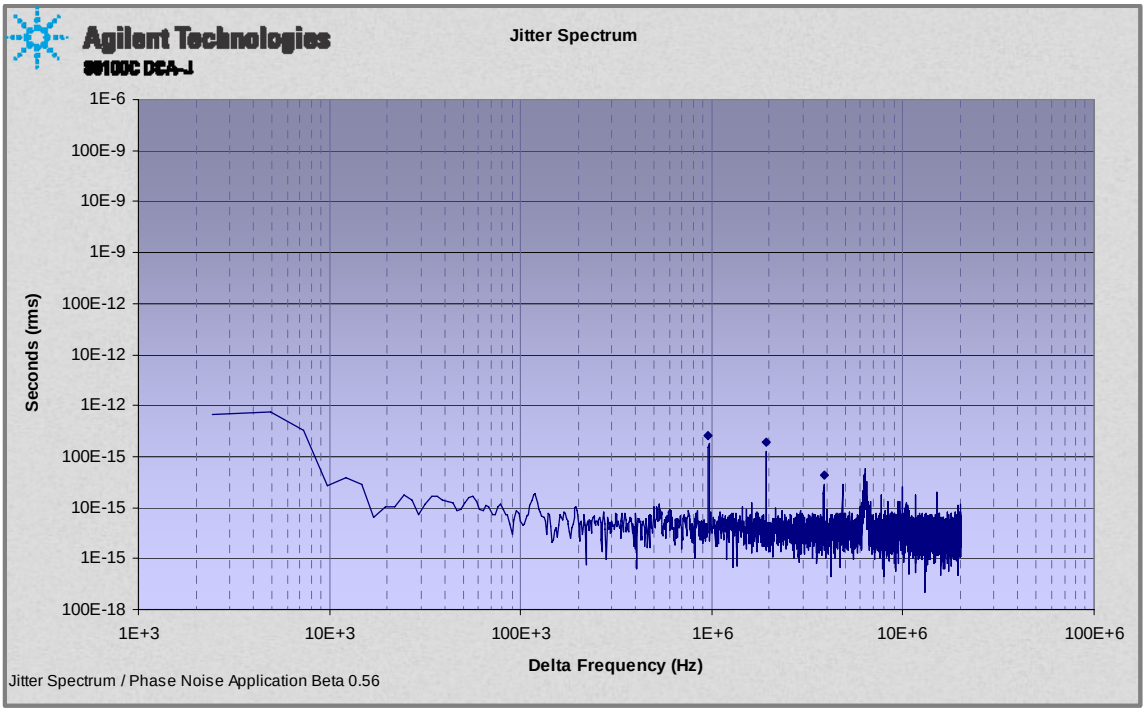
B. Several things will now happen:
   1 The application measures the loop response of the 83496B clock recovery circuit as it is locked to the signal being measured (if *Measure Loop* is set to 1). This data is recorded in the spreadsheet under tab “dataBW”.

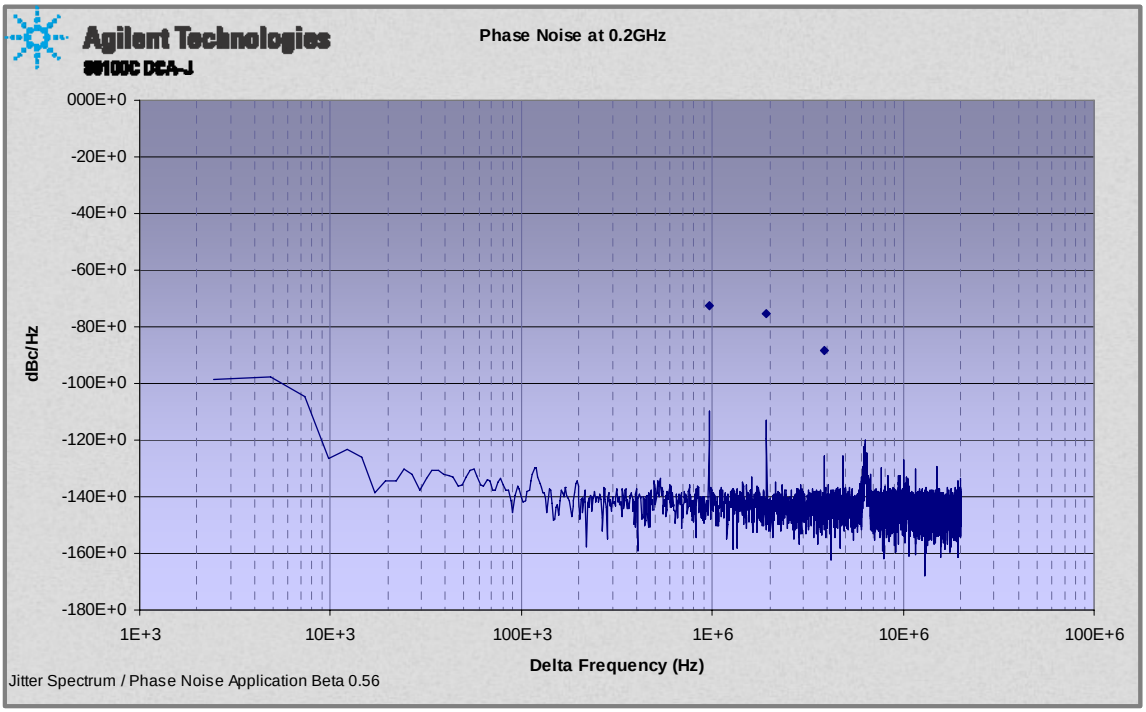


The above plot is essentially the response of the 83496B to an internally generated step (within the loop). This response is then used to back out the effects of the 83496B on the measured results.

   2 The Phase Error (output of the phase detector in the clock recovery phase locked loop) will be recorded in the spreadsheet under tab “DATA”. The information provided here is useful only to the extent that it indicates that the loop response has been measured. There is no information relative to the signal being measured on this sheet. Each measurement is based on a 40 Ms/s or 4 Ms/s time record of 12288 points. Results are displayed as a function of time or transformed to be displayed in the (jitter) frequency domain. Because the loop response is known, it is possible to remove its response as well as view the signal from the perspective of the input to the 83496B or the output of the internal phase detector.
   3 The most common view is the jitter spectrum (jitter in seconds versus jitter frequency) and phase noise (jitter power relative to the total signal power, normalized to a 1 Hz bandwidth, again versus jitter frequency. This is viewed

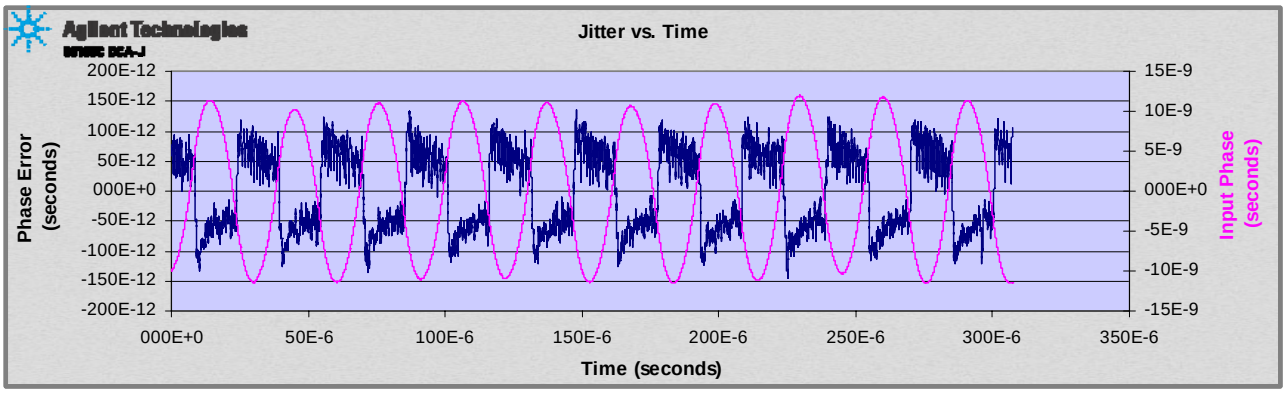
by selecting the Jitter Spectrum tab. The displayed result allows either the jitter spectrum or phase noise to be displayed.





A toggle button (not shown here) allows switching between the jitter spectrum and phase noise displays. If the toggle button is not displayed on the graph, clicking on any of the spreadsheet cells should allow the button to be displayed.

4 The results can also be observed in the time domain. When the TIME tab is selected, two measurements are presented. Jitter versus time is a dual display. The pink trace is the phase modulation seen at the input of the 83496B phase detector. This plot helps indicate how the 83496B can track jitter and remove it from a general waveform analysis using the 86100C. Thus the pink input phase error is a measure of the "total" jitter observed by the 83496B. Note that since phase is the integral of frequency, if triangle shaped SSC frequency modulation were present, this display would be a parabolic shaped phase deviation. Viewing the input phase in the jitter domain provides an important troubleshooting capability. If there are ever phase transients, for example when a PLL loses synchronization or exceeds its allowable phase range, the phase "glitch" can be observed directly in the pink input phase trace. The blue phase error trace is an indication of the actual signal that the 86100C/83496B measurement system is observing. Below is the jitter vs time plot for a signal with SSC:



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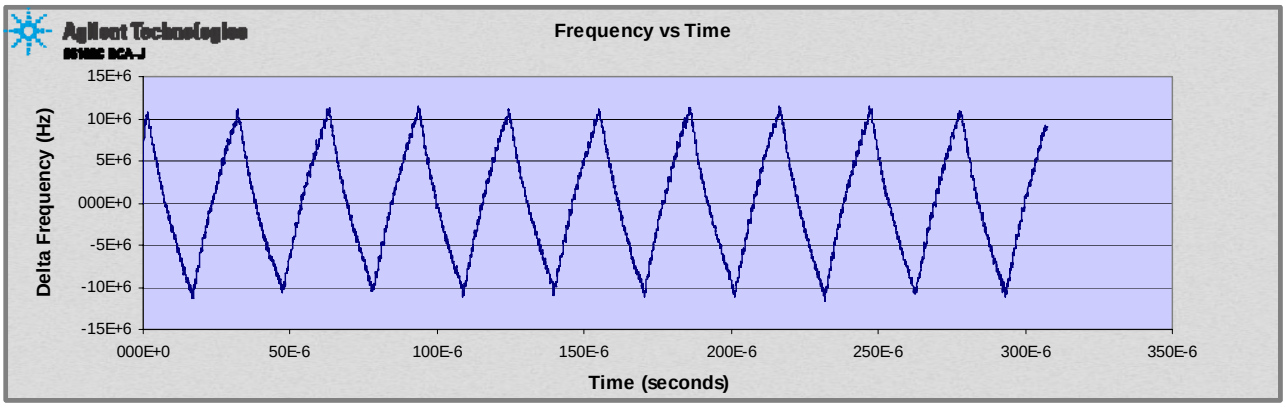
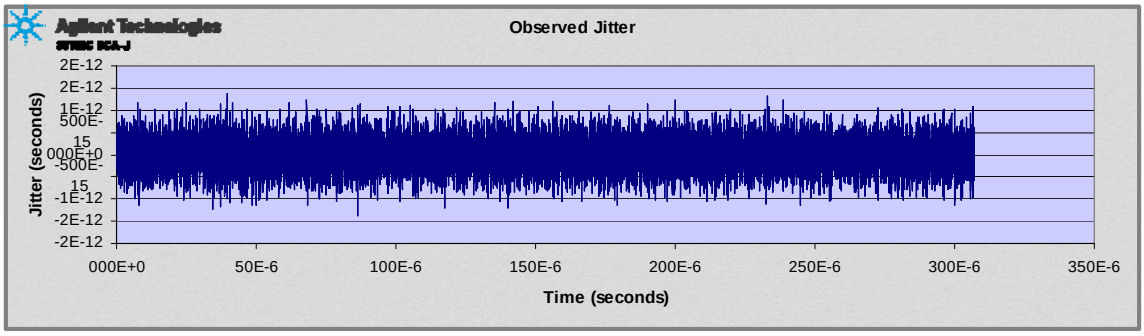
5 The blue trace on this graph helps indicate how the 83496B can track jitter and remove it from a general waveform analysis using the 86100C. Thus the pink input phase error is a measure of the "total" jitter observed by the 83496B. The blue phase error indicates the residual jitter not tracked by the 83496B. It is simply an indicator of how "hard" the 83496B phase lock loop is working to track the incoming signal. If the input phase and the phase error were similar, it would indicate that the 83496B PLL is not tracking the input signal. Note that the axes for the input phase error are orders of magnitude larger than the vertical axis for the phase error.

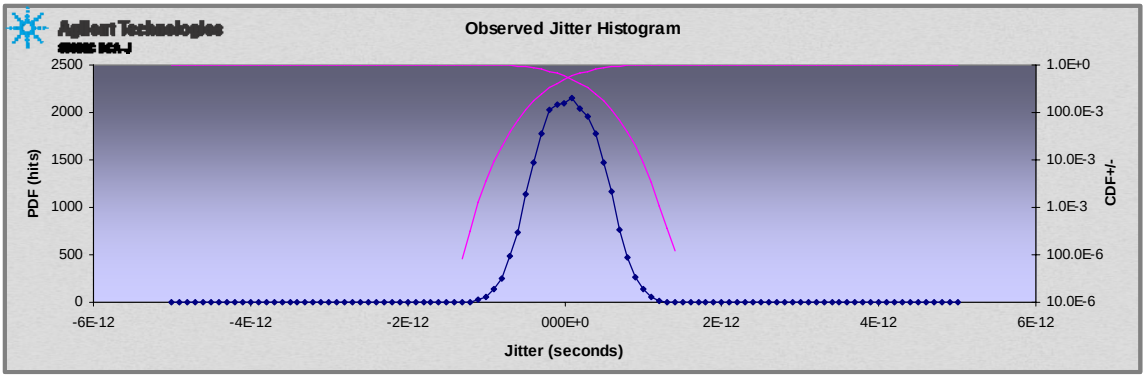
6 The second plot for the TIME tab is delta frequency versus time. This simply displays the difference in frequency, compared to the ideal (jitter free)

frequency, of the input signal as a function of time. The example below is for the signal with SSC present.



7 The HISTOGRAM tab displays the test signal as it would be observed having gone through the post-processing function configured in the setup page. The post processing allows the measured signal to be passed through two "virtual" PLLs with a fixed transport delay between them. The loop bandwidths of the virtual PLL's can "clean up" the jitter, but the clean up is affected by any time delay the signal experiences traveling from one PLL to the other. There are two displays in this tab. The observed jitter, measured in seconds, can be displayed as a function of time. This is the upper plot. The probability density (how often the signal reaches a given jitter magnitude) is displayed in the lower plot.





The pink traces of the histograms represent the cumulative distribution functions for each half of the histogram.

Note that the histogram result is only available when post processing is enabled.

IX Interpreting the results

There is a wealth of information available from the jitter spectrum and phase noise measurement results but what is of interest to the user depends on the particular signal being measured and issues being investigated. Some of the common insights are listed here:

- *Phase Noise and Jitter Spectrum Charts*

These charts have the same x-axis and plot shape but have differing vertical axes. The vertical axis for the Phase Noise plot is in dBc/Hz and that chart looks like the typical phase noise plot. The vertical axis for the Jitter Spectrum chart is jitter in Seconds RMS.

As already noted, periodic jitter is displayed as discrete spectral lines. However, there can be spurious spectral lines that are artifacts of the measurement process. At this point in time the jitter spectrum and phase noise measurement is not synchronized with the data pattern so it is possible some pattern effects can be seen in the measurement results. When evaluating a data signal composed of an even length repeating pattern it is possible for a small spike to be present if the difference between the pattern repetition rate (data rate/ pattern length) and a harmonic of the sample rate (4 Mb/s or 40 Mb/s) falls within the frequency measurement window. For odd length repeating patterns two small spikes can occur, one where the difference between the pattern repetition rate and a harmonic of the sample rate falls within the frequency measurement window and another at half that frequency. For example:

- Data Rate = 9.953 Gb/s
- Sample Rate = 40 MHz

- Frequency Measurement Window = 3kHz to 20 MHz
- Pattern Length = 127 Bits (odd)
- Pattern Repetition Rate = (9.953Gb/s)/127 bits = approx 78.4 Mhz
- Pattern Repetition/2 = 39.2 MHz
- Measurement spur possible at 80 MHz-78.4 MHz = 1.6 MHz
- Measurement spur possible at 40 MHz – 39.2 MHz – 800 kHz

The Results Page

Most of the results produced by the JSPN application are graphical. However, some results are numerical. Specifically, the spectrum can be analyzed to determine its contribution to the overall random, deterministic, and total jitter of a signal. This is achieved by integrating the jitter spectrum over user defined bandwidths (defined above in Post Processing). The results page provides a summary of the numerical measurements that JSPN can make.

Time of Measurement	##########					
Revision	Beta 0.57					
Left Module	83496B					
Right Module	86112A					
Data Rate	5.000E+9					
Loop Bandwidth	100.000E+3					
Transition Density	0.9984					
Input	EINV					
Post Processing						
Frequency filter	PLL1	PLL2	Difference			
2.00E+6	4.65E+6	9.40E+6	1.00E+0			
10.00E+3	1.00E+9	1.00E+9	12.00E-9			
1.50E+6	3.99E+6	8.06E+6				
Integrated Jitter	TJ (rms)	DJ (rms)	RJ (rms)	Spec	Pass/Fail	
Integral f1 to fmax	138.21E-15	16.00E-15	137.28E-15			
Integral f2 to fmax	52.46E-15	11.16E-15	51.26E-15			
Difference f1 to f2	127.86E-15	11.46E-15	127.35E-15			
Highest Peak						
Frequency	161.308E+3					
Jitter (rms)	11.46E-15					
Jitter (p-p)	32.43E-15					

Saving results

Since the JSPN application is based on a spreadsheet, saving the spreadsheet file will also save the current measurement results. However, the spreadsheet application is a very large file. Also, as the majority of the measurement information is graphical in nature, it can be complicated to transport spreadsheet based graphics to other applications. The memory and complexity problems of measurement result storage are solved through the Save Results function found on the Setup page. When this is executed, the graphic displays from the Jitter Spectrum, Time, and Histogram pages are saved as a file including the graphic images and does not include the supporting spreadsheet information, significantly reducing the file size. In addition to the graphics, the information from the Results page is also recorded. (Note that marker functions used on graphics on spreadsheet pages are not functional on the saved results images).

Verifying system operation

As long as the 83496B is capable of locking onto the signal being tested, the JSPN application should provide good measurement results. The JSPN application performs best with narrow loop bandwidth settings for the 83496B. However, complicated signals may require the 83496 to have a wider loop bandwidth to achieve lock. Use the lowest loop bandwidth for which a lock condition can be achieved.

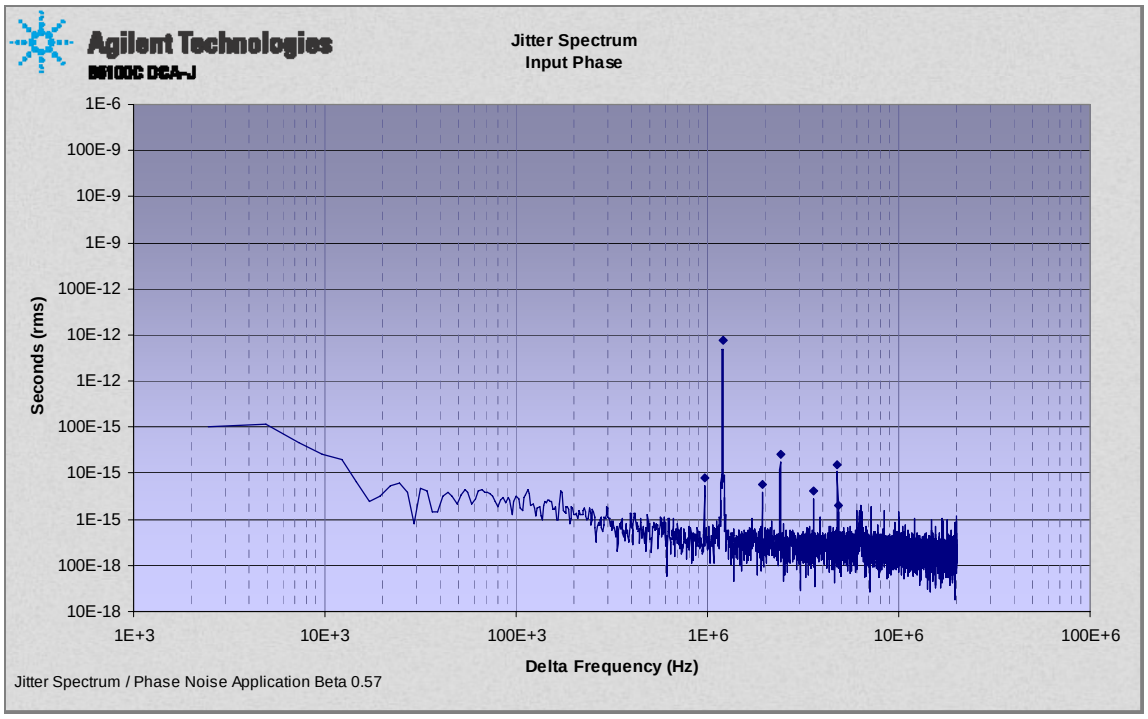
Verification of operation can be achieved by measuring a high quality signal generator producing a simple clock or sinusoid. Use of a high quality generator should yield a signal with low jitter spectrum noise (and low phase noise) providing an indication of the JSPN system ability to observe low jitter signals. Some examples of signal generators that might be used include the Agilent 8257D or 8267D. Any generator capable of producing a clock like signal at GHz frequencies will work, but signals with reduced spectral purity will result in higher jitter noise results. Basic system operation can still be confirmed. The ability to also produce a specific level of periodic jitter at a specific frequency will also help verify system operation.

In the following example, a 2.5 GHz clock signal from an Agilent 8267D is measured. The Signal Studio software application is used to generate 0.1 UI of periodic jitter at 1.2 MHz.

The following is the JSPN configuration:

Data rate: 5E+09 (double the frequency when measuring a clock)
Loop BW: 100000
Input: ELEC (single ended input to the 83496)

When the application is run, including setting up the clock recovery and measuring the jitter, the following jitter spectrum is observed:



The 8267D has extremely low phase noise, thus the jitter spectrum is quite low, under 1 fs above 300 kHz. The periodic jitter is seen as several tones, with the dominant tone at 1.2 MHz. There are also tones at 2.4 MHz and 3.6 MHz. These represent harmonic distortion components of the desired 1.2 MHz periodic jitter. Two important points need to be made. Note that the harmonic distortion components are several orders of magnitude smaller than the main tone (the y axis is logarithmic). Also, the very low phase noise of the source allows the distortion tones to be observed. More common digital communications signals often have jitter noise that would completely obscure these tones. In addition to the 1.2 MHz series of tones, there are also tones at approximately 950, 1900, and 2850 kHz. These are tones from the switching power supply in the 83496B. Again, the ultra low jitter of the 8267D source allows these spurious tones to be observed.

The magnitude of the 1.2 MHz tone can be confirmed by going to the results page.

Time of Measurement	39210.83
Revision	Beta 0.57
Left Module	86106B
Right Module	83496B
Data Rate	5E+09
Loop Bandwidth	100000
Transition Density	0.9953
Input	ELEC
Post Processing	

Frequency filter	PLL1	PLL2	Difference
2000000	4650000	9400000	1
10000	1E+09	1E+09	1.2E-08
1500000	3990000	8060000	

Integrated Jitter	TJ	DJ	RJ
Integral f1 to fmax	7.49E-12	7.49E-12	5.08E-14
Integral f2 to fmax	4.05E-14	3.06E-14	2.65E-14
Difference f1 to f2	7.49E-12	7.49E-12	4.33E-14

Highest Peak	
Frequency	1200011
Jitter (rms)	7.49E-12
Jitter (p-p)	2.12E-11

The jitter frequency is measured at 1200011 Hz vs. an expected value of 1200000 Hz. The magnitude of the jitter is 7.49 ps rms and 21.2 ps peak-peak. The system was set to produce 0.1 UI pp of sinusoidal jitter. At 5 Gb/s, 1 UI is 200 ps. Thus the 21 ps value is within 5% of the expected 20 ps pp value.

The best way to gauge the magnitude of the random jitter, represented by the noise floor of the jitter spectrum, is to integrate it over a specific bandwidth. The maximum frequency range of the application is 20 MHz. The integration limits are defined as part of the post processing system and shown as Filter 1 and Filter 2 in the results page (and are used to set the integration limits whether or not the signal is processed through the virtual PLL's). In this setup the F1 filter value is 10 kHz, F2 is 1.5 MHz. The integrated jitter from 10 kHz to 20 MHz is 50.8 fs, from 1.5 MHz to 20 MHz is 26 fs, and from 10 kHz to 1.5 MHz is 43 fs. This is all noted in the results table above.

When the system is verified with a signal other than the one described above, the results will obviously be different. Results will depend on the quality of the source and the precision to which periodic jitter can be produced. As noisier sources are used, the integrated jitter spectrum will be larger. However, the example given should provide some levels that can be expected for specific conditions as well as an indication of the lower regions of what can be observed.

Appendix A: Transient/Glitch Capture Mode (Advanced)

There may be situations where the signal being tested is normally well behaved but occasionally has a fault creating a significant phase error component. An example where this may occur is when the phase detector in a clock multiplier circuit phase "wraps" (phase exceeds +/- π). In this case it is desirable to evaluate the signal over a long period of time and record the measurement only when the large phase error occurs. The JSPN Application can help to measure this phenomenon in the Glitch Capture Mode.

To run in the Glitch Capture Mode follow the General Settings in section VII and then the instructions below:

A. *Threshold*: This value, which is (peak phase error)/sigma, sets the threshold to trigger saving data and recording a jitter spectrum and phase noise measurement Thus a transient event will be captured if the phase error exceeds the standard deviation of the overall phase error by the threshold value. To operate in the Glitch Capture Mode some trial and error may be required to determine the ideal threshold value. Setting "threshold" too low may cause the instrument to trigger on events that are not significant. Setting the threshold too high may result in the phase transient never being captured. A typical starting point would be a threshold of 2, which would cause the system to trip when the phase error is double the overall standard deviation. If the system achieves the maximum measurement, the system will stop without having been triggered by a phase transient. The threshold should be decreased. If the system trips on signals other than the event that is being sought, the threshold value should be increased.

B. *Measure Loop*: This defines if the loop response of the 83496B clock recovery module, as locked to the signal being evaluated, will be measured. If the 83496B clock recovery module is already locked to the signal being evaluated and a standard Jitter spectrum and phase noise measurement has already been run, the JSPN Application has evaluated and recorded the loop response and further measurements of the loop are not required. If that is the case, set this value to 0 so further loop measurements are not made, enabling the application to run faster. If the loop has not yet been evaluated or has been re-locked since the last time the loop was evaluated, set this value to 1 so the loop response can be measured.

C. *Max Measurements*: Sets the maximum number of measurements the application will make as it looks for a phase error that meets the *Threshold* criteria. Setting this value to a large number will allow the application to make many measurements as it looks for a phase error that meets the *Threshold* you have set above. However, the application will not stop until it has either:

   1 found a phase error that meets the *Threshold* set above, or

   2 measured the signal the number of times set for *Max Measurements*

   Notes:

   - A high *Threshold* setting combined with a large value for *Max Measurements* will result in a long test time.
   - If the threshold is reached the Phase Error chart will show the result of only the last measurement (where the threshold was reached) and the Phase Noise and Jitter Spectrum charts will be averaged over all the measurements taken.

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Appendix B Averaging the Measurement in the Frequency Domain

To minimize noise in the frequency response plots you can set up the measurement to average in the frequency domain (the phase error in the time domain will not be averaged).

To average in the frequency domain follow the General Settings in section VII and then the instructions below:

A. *Threshold*: This sets the phase error threshold to trigger the saving data process and records a jitter spectrum and/or phase noise measurement. Set to a large number such as 100, this state is likely never reached, allowing the desired number of averages to be completed before the data is recorded and processed.
B. *Measure Loop*: This defines if the loop response of the 83496B clock recovery module, as locked to the signal being evaluated, will be measured. Set to 1 so the loop response will be measured.
C. *Max Measurements*: Sets to the number of averages desired.

Appendix C Measuring signals below 50 Mb/s

Note that the minimum data rate supported by the 83496B clock recovery module is 50 Mb/s, indicating the minimum data rate supported by the JSPN Application is 50 Mb/s or a 25 MHz clock. However, depending on your data pattern, you may be able to lock the clock recovery module to a slower data rate or slower clock.

A. A 1011001 pattern at 25 Mb/s looks just like a 11001111000011 pattern at 50 Mb/s. A clock signal is just a special case where the pattern is a repeating 101010…. If you have a signal you need to evaluate that is below the minimum rate (50 Mb/s) supported by the 83496B you can try to lock the clock recovery module to that signal by telling the clock recovery module the signal is 2, 3 or 4 times faster than the actual data rate.
B. The clock recovery circuit then just considers each bit in the pattern to be 2, 3 or 4 consecutive identical bits. Provided the clock recovery module can lock to the signal, the jitter spectrum and phase noise measurement results will not be affected by this approach.